

FIG. 1

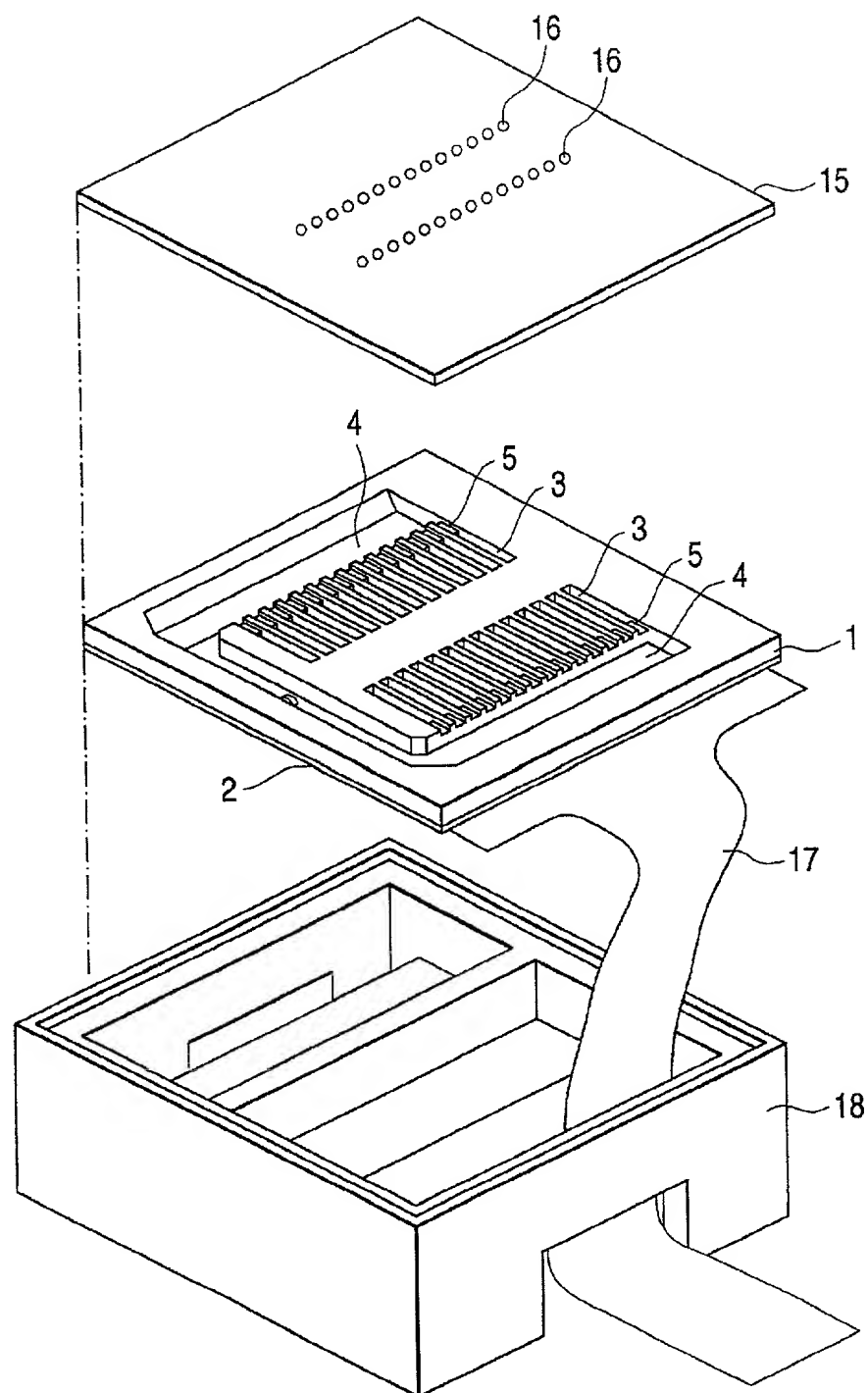


FIG. 2(A)

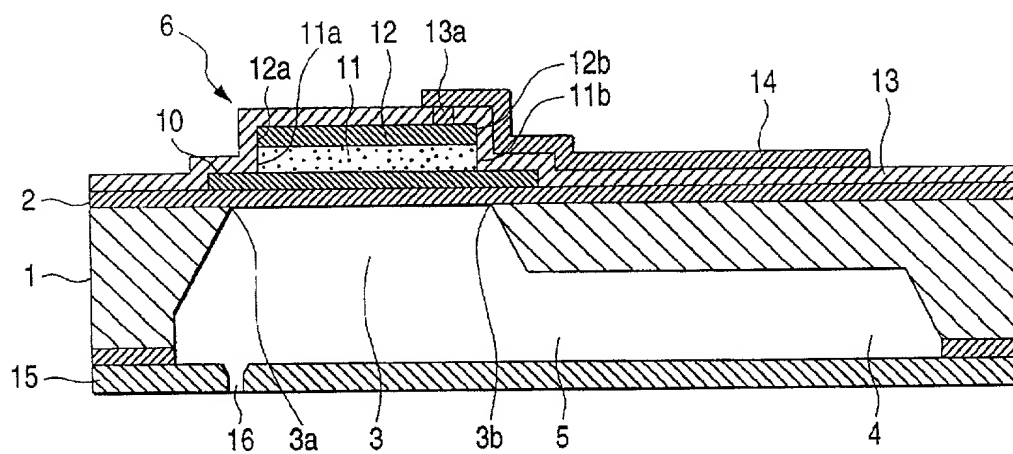


FIG. 2(B)

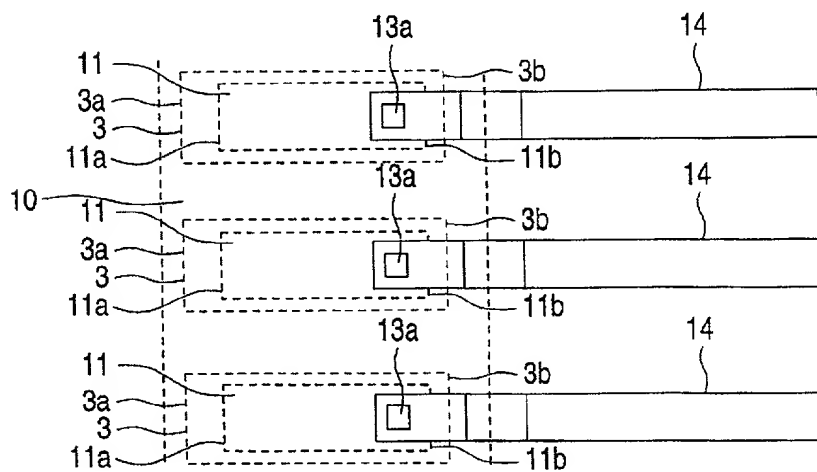


FIG. 3(A)

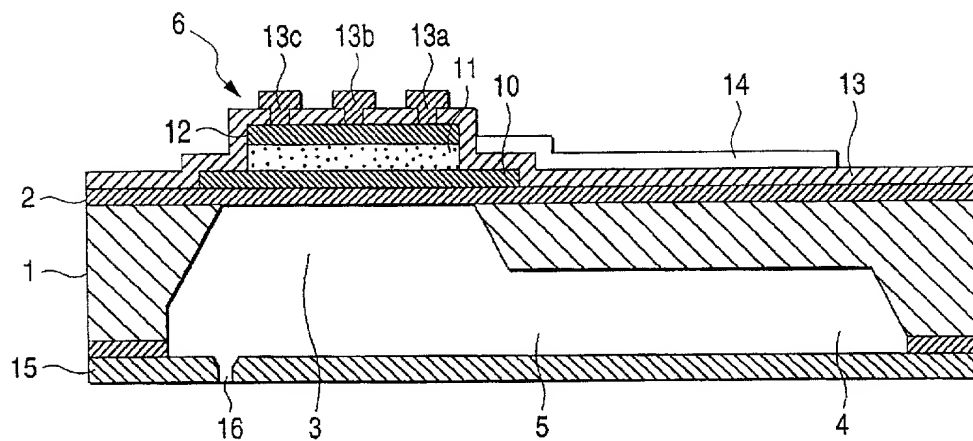
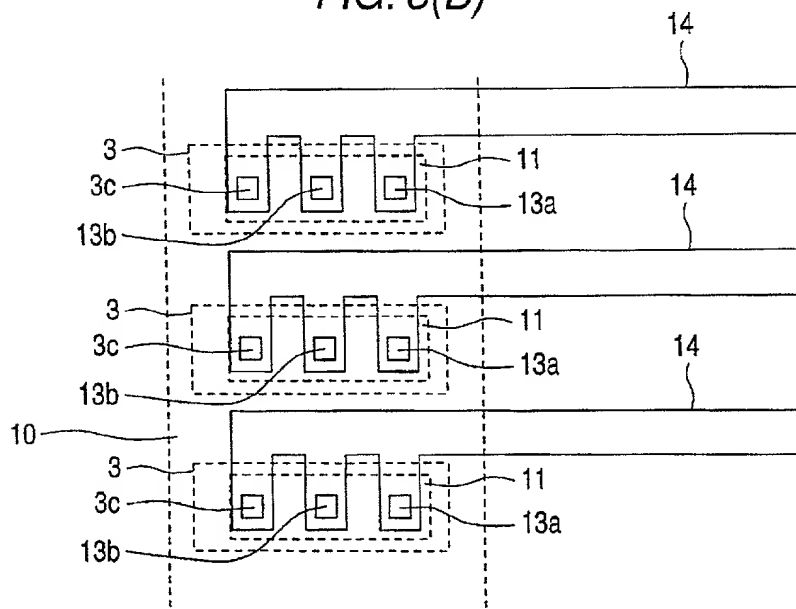


FIG. 3(B)



A cross-sectional view of a semiconductor device. The device features a substrate (1) with a trench (2) and a gate stack (3) on top. The gate stack includes a gate oxide layer (1), a gate polysilicon layer (2), and a gate dielectric layer (3). The source/drain region includes a source/drain polysilicon layer (4) and a source/drain dielectric layer (5). The trench is filled with a material (6). Dimensions  $\Delta L$  and  $\Delta L'$  are indicated.

A cross-sectional view of a semiconductor device showing two unit cells. The device consists of a substrate 1 with a base layer 3 and a patterned layer 16. On top of the patterned layer 16, there are two identical structures. Each structure includes a layer 11, a layer 12, and a layer 13. A central layer 14 is positioned between the two unit cells. The width of the central layer 14 is indicated by  $\Delta L''$ , and the width of the side layers 12 and 13 is indicated by  $\Delta L'$ .

FIG. 5 - I

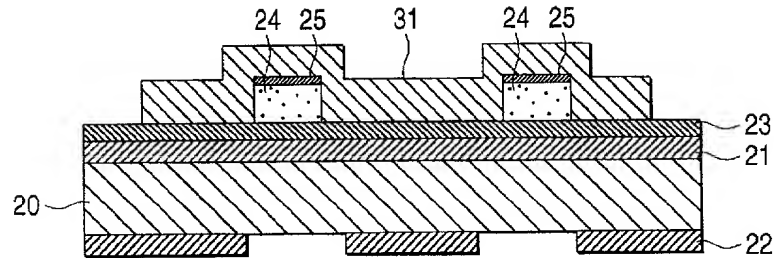


FIG. 5 - II

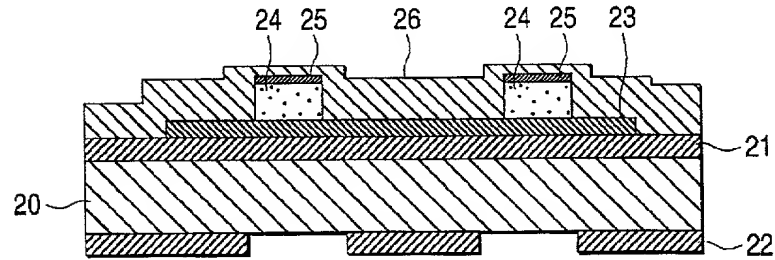


FIG. 5 - II'

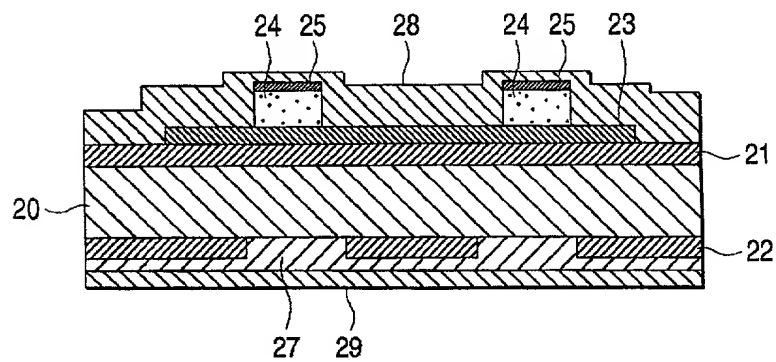


FIG. 6 - I

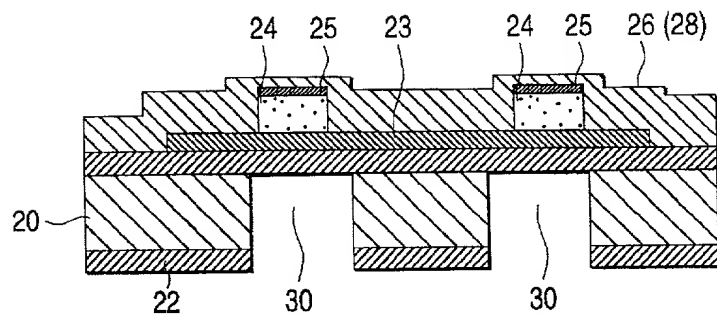


FIG. 6 - II

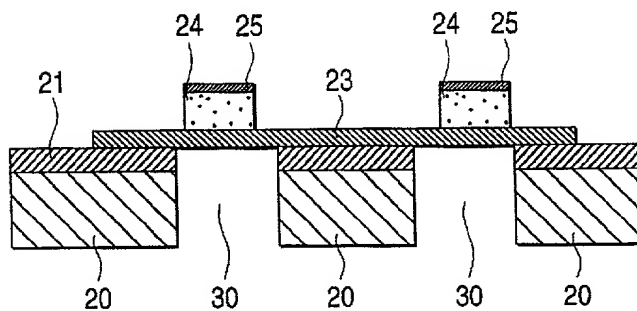


FIG. 6 - II'

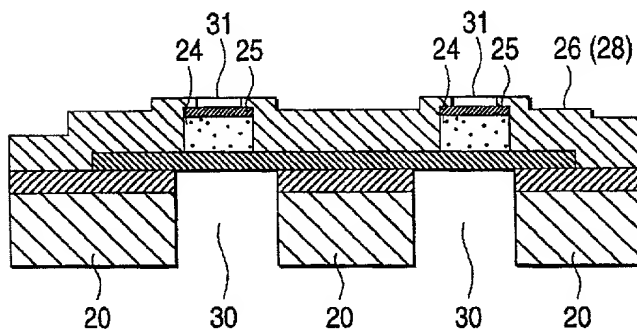
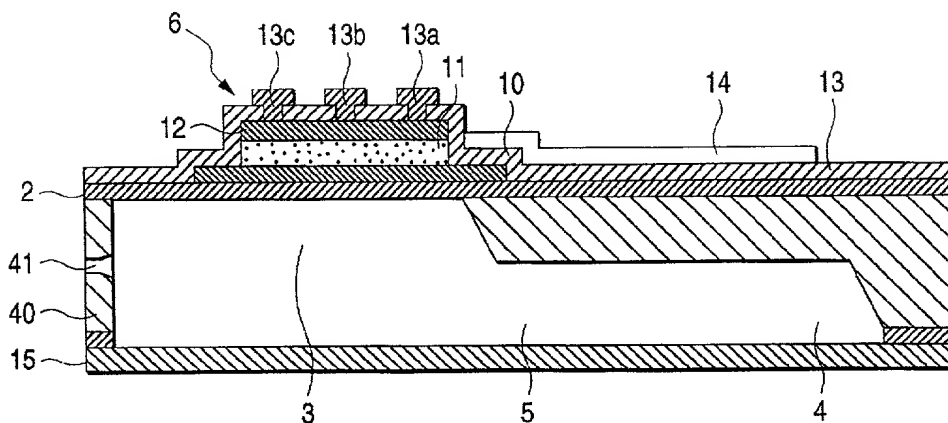


FIG. 7



**FIG. 8**  
PRIOR ART

